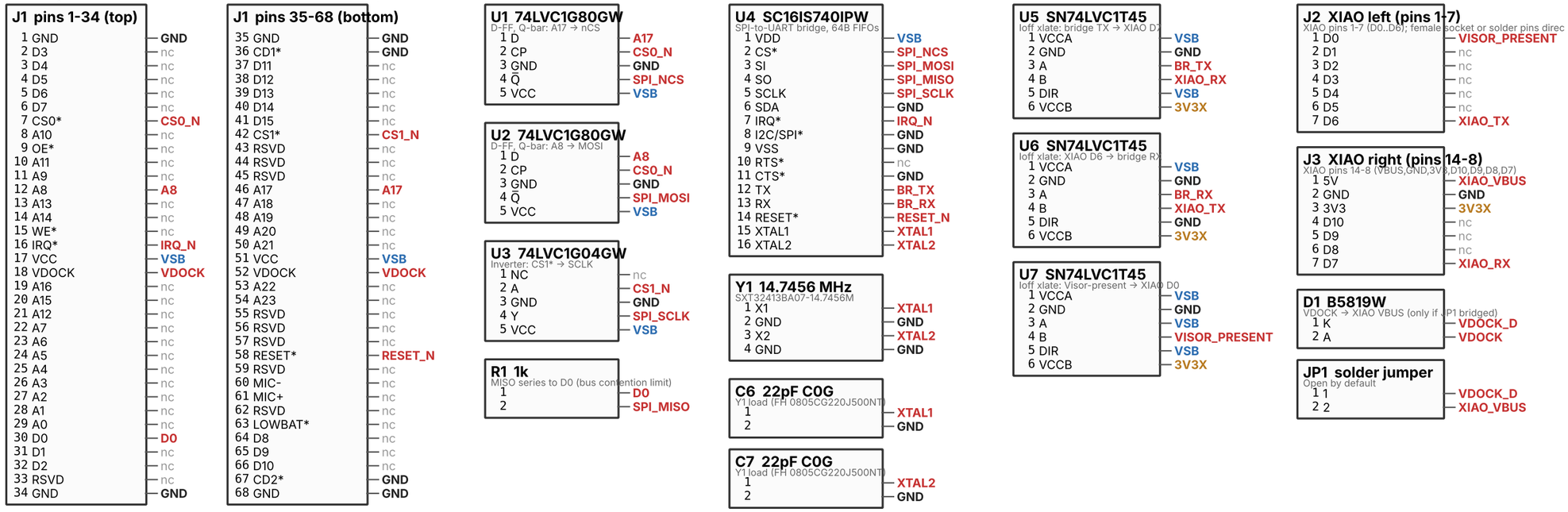
VisorMesh SB-LoRa v0.1 - Springboard MeshCore companion module

Net-label schematic: pins with the same net name are connected. Blue = Springboard VCC domain (VSB), amber = XIAO 3V3 domain (3V3X).

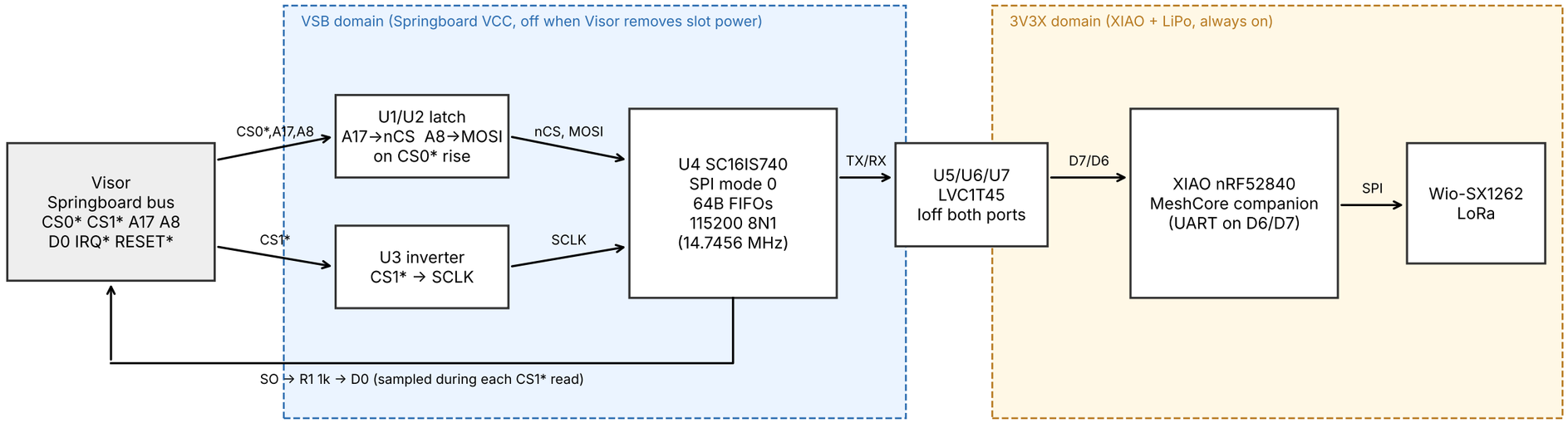
J1 Springboard 68p straddle: Hirose IC1HA-68RD-1.27SH(51), hand-solder



Passives

C1	1uF	VSB	-	GND	VSB bulk
C2	100nF	VSB	-	GND	U1 decoupling
C3	100nF	VSB	-	GND	U2 decoupling
C4	100nF	VSB	-	GND	U3 decoupling
C5	100nF	VSB	-	GND	U4 decoupling
C8	100nF	VSB	-	GND	U5 VCCA
C9	100nF	3V3X	-	GND	U5 VCCB
C10	100nF	VSB	-	GND	U6 VCCA
C11	100nF	3V3X	-	GND	U6 VCCB
C12	100nF	VSB	-	GND	U7 VCCA
C13	100nF	3V3X	-	GND	U7 VCCB
C14	1uF	3V3X	-	GND	3V3X bulk
R2	100k	3V3X	-	XIAO_RX	XIAO RX idle-high pull-up
R3	100k	VSB	-	BR_RX	Bridge RX idle-high pull-up
R4	100k	VISOR_PRESENT	-	GND	Visor-present pull-down

Theory of operation



Bus protocol (identical address bits to springSD, so its 68k SPI routines carry over):

- Any CS0* access latches A17 and A8 on the rising edge of CS0*. U1/U2 are Q-bar outputs, so nCS = NOT A17 and MOSI = NOT A8. To assert chip select, touch csSlot0 with A17=1; to send bit b, touch csSlot0 with A8 = NOT b (A17 kept at 1).
- Any CS1* read produces one SCLK pulse (high while CS1* is low). The SC16IS740 samples SI on the rising edge (SPI mode 0) and shifts SO on the falling edge; read bit 0 of the 16-bit word returned by the CS1* access to get MISO.
- SC16IS740 register byte: bit7 R/W (1=read), bits6:3 register address, bits2:1 channel (00), bit0 unused.
- SC16IS740 IRQ* is open-drain straight onto Springboard IRQ* (the Visor provides the pull-up). RESET* follows the slot RESET*.

Power-domain rules:

- Only U5-U7 touch both domains. SN74LVC1T45 ports go high-impedance when either VCC is 0 V, so pulling the module, a Visor sleep/LOWBAT power cut, or a flat LiPo never back-powers the other side. R2/R3 keep both UART RX lines idle-high.
- U7 reports slot power to XIAO D0 (VISOR_PRESENT, high = Visor powering the slot). Firmware can gate UART output on it.
- Springboard VCC load: U1-U4 + VCCA of U5-U7, a few mA active, under 100 mA. Put the SC16IS740 in sleep (IER[4]) when idle to stay inside the 100 uA standby budget.
- JP1 (default open) routes VDOCK (4.75-6.2 V, dock only) through D1 into the XIAO 5V pin so the XIAO charger can top up the LiPo in a charging dock. Do NOT bridge JP1 if you will ever plug USB-C in while docked: VDOCK would back-feed the USB host.